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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/815,934	04/02/2004	Shinya Takyu	02887.0274	9440

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EXAMINER	
KEBEDE, BROOK	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 09/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/815,934	TAKYU ET AL.
	Examiner	Art Unit
	Brook Kebede	2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,3,12 and 13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,3,12 and 13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/21/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 2, 3, 12, and 13 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 17 and 18, 20 and 21of copending Application No. 10/808,298 in view of Sugino et al. (EP/ 1107299).

Re Claims 2, 3, 12 and 13, the claimed subject matter of the instant application is already claimed in claims 15-25 of the co-pending U.S. Application No. 10/808,298 except for the limitation "providing a groove having a thickness equal to or larger than a finishing thickness on a first surface of a semiconductor wafer on which a semiconductor element is formed; affixing a pressure sensitive adhesive (PSA) tape onto the first surface of the semiconductor wafer in which the groove is formed; reducing the thickness of the semiconductor wafer by processing a second surface opposite to the first surface of the semiconductor wafer onto which the PSA tape is affixed, so as to separate the semiconductor wafer into a plurality of semiconductor chips on which the semiconductor element is formed; affixing an adhesive layer onto an entire rear surface of the separated semiconductor wafer; cutting the adhesive layer so as to separate the

adhesive layer for each of the semiconductor chips; and peeling off the PSA tape from the semiconductor wafer while fixing the semiconductor wafer under suction by use of a porous member segmented into at least two sucking areas ."

Sugino et al. disclose a manufacturing method of a semiconductor device, comprising: providing a groove (2) having a thickness equal to or larger than a finishing thickness on a first surface of a semiconductor wafer (1) on which a semiconductor element is formed (see Fig. 1); affixing a pressure sensitive adhesive (PSA) tape (10) onto the first surface of the semiconductor wafer (1) in which the groove is formed (see Fig. 2); reducing the thickness of the semiconductor wafer (1) by processing a second surface opposite to the first surface of the semiconductor wafer (1) onto which the PSA tape is affixed (see Fig. 3), so as to separate the semiconductor wafer into a plurality of semiconductor chips (see Fig. 4) on which the semiconductor element is formed; affixing an adhesive layer onto (20) an entire rear surface of the separated semiconductor wafer (see Fig. 4); cutting the adhesive layer so as to separate the adhesive layer for each of the semiconductor chips (3) (see Fig. 5); and peeling off the PSA tape from the semiconductor wafer while fixing the semiconductor wafer under suction by use of a porous member segmented into at least two sucking areas (see Figs. 1-6 and related text in Pages 2-6) in order to form an appropriate amount of adhesive layer on the back of extremely thin chips and that enables to avoid chip breakage, chip cracking or package cracking.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide the co-pending Application No. 10/808,298 with providing a groove having a thickness equal to or larger than a finishing thickness on a first surface of a semiconductor wafer on which a semiconductor element is

formed; affixing a pressure sensitive adhesive (PSA) tape onto the first surface of the semiconductor wafer in which the groove is formed; reducing the thickness of the semiconductor wafer by processing a second surface opposite to the first surface of the semiconductor wafer onto which the PSA tape is affixed, so as to separate the semiconductor wafer into a plurality of semiconductor chips on which the semiconductor element is formed; affixing an adhesive layer onto an entire rear surface of the separated semiconductor wafer; cutting the adhesive layer so as to separate the adhesive layer for each of the semiconductor chips; and peeling off the PSA tape from the semiconductor wafer while fixing the semiconductor wafer under suction by use of a porous member segmented into at least two sucking areas as taught by Sugino et al. in order to form an appropriate amount of adhesive layer on the back of extremely thin chips and that enables to avoid chip breakage, chip cracking or package cracking (see Sato et al. Abstract also).

This is a provisional obviousness-type double patenting rejection.

Response to Arguments

3. Applicants' arguments with respect to claims 2, 3, 12 and 13, i.e., rejections under provisional obviousness-type of double patenting, have been considered but are moot in view of the new ground(s) of rejection.

Remarks

4. Applicants remark with respect of IDS that was filed on October 21, 2004 is noted. Accordingly, relevant portion the information disclosure statement is being considered by the examiner and a copy of PTO-1449 is attached hereto.

Conclusion

5. **THIS ACTION IS MADE NON-FINAL.**

Correspondence

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (571) 272-1862. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brook Kebede

Brook Kebede
Examiner
Art Unit 2823

BK
September 4, 2005